The present invention as claimed in independent claim 1 is directed to a method for providing trench isolation in a semiconductor device. An etching mask pattern is formed on a semiconductor substrate to expose a predetermined region of the semiconductor substrate. The exposed semiconductor substrate is then etched, using the etching mask pattern as an etching mask, to form a trench. An insulating layer is formed over the trench and nearby regions, the insulating layer filling the trench. A high-temperature oxide (HTO) layer is provided on the insulating layer, the HTO layer being formed at a temperature of 700C to 800C. In this manner the underlying insulating layer is densified during formation of the HTO layer. The HTO layer and the insulating layer are planarly etched down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench. The exposed etching mask pattern is then removed. (emphasis added)

In this manner, the method of the present invention as claimed in claim 1 provides for densification of the insulating layer (see for example, reference 23 of FIG. 1F), during formation of the HTO layer (reference 24 of FIG. 1F) at a temperature of 700C - 800C, Accordingly, there is no need to perform a subsequent, additional annealing process in order to densify the underlying insulating layer, which otherwise could lead to a number of process limitations, as specified in the present application as filed at page 2, lines 2 - 23.

The current Office Action maintains the rejection of independent claim 1 on the basis that Laparra and Park disclose all steps of the claim except for forming the "material layer" at a "temperature of 700C - 800C". The applicants note that independent claim 1 states specifically that an "HTO layer" is formed at this range of temperatures, and not just any "material layer", as stated in the Office Action.

The current Office Action further takes the position that Shin and Park teach that the HTO and LP-TEOS processes are interchangeable, and should therefore be considered as "art equivalent layers" (Office Action of March 26, 2003, page 3, paragraph 4). The applicants

respectfully disagree with this assertion, and provide the following discussion regarding the differences between the two processes.

Chemical Vapor Deposition (CVD) processes, used for forming a silicon dioxide layer, can be classified as atmospheric-pressure-CVD (AP-CVD) and low-pressure CVD (LP-CVD), in terms of the pressure under which the process takes place. AP-CVD is performed at low temperature, but has poor step coverage. LP-CVD is performed at high temperature, and has heightened step coverage. When plasma is used in the LP-CVD process, for example in the plasma-enhanced-CVD process (PE-CVD), deposition can be performed at a lower process temperature.

The composition of the resulting silicon oxide formed as a result of the various CVD processes described above can vary according to process source gasses used, process pressure and process temperature. For example, the LP-TEOS-based layer mentioned in Park and Shin, refers to a silicon oxide layer, formed in the LP-CVD process, using TEOS as a source gas. The LP-TEOS formation process is performed at a high temperature, because the LP-CVD deposition process is used.

On the other hand, the "HTO layer", stated in claim 1 of the present invention, is a silicon oxide layer that is formed at a high temperature, using a source gas of silane (SiH_4) gas or dichlorosilane (SiH_2Cl_2) gas.

Based on the above, it is apparent that both the LP-TEOS-based layer and HTO-based layer are representative of silicon oxide layers formed using a LP-CVD process, and are therefore formed at a high temperature. However, the resulting oxide layers are entirely different in composition, since the source gases used for in their formation are different. For this reason, claim 1 specifically refers to an "HTO layer", namely, a "high-temperature *oxide*" layer, that is, specifically, a term of art that referring to an oxide layer formed using a silane (SiH_4) or dichlorosilane (SiH_2Cl_2) source gas, and not merely to just *any* oxide layer that is formed by high

temperature, *i.e.* any high-temperature *process* that results in oxide layer formation, for example TEOS.

It is further submitted that replacement of the HTO layer with an LP-TEOS layer for the purpose of densification would be undesirable, as formation of the LP-TEOS layer at such a high temperature of 700C- 800C, as claimed in claim 1 would result in the penetration of carbon into adjacent active regions of the device. Remarks related to the issue were previously provided by the applicants in the Amendment After Final, filed on December 20, 2002, at page 5, paragraph 3:

> The Applicants note that in the TEOS process, carbon introduced in the source material tetraethosiloxane, $Si(OC_2H_5)_4$ has a high degree of penetration into the active area at the high temperature of "not less than 650C" stated in Shin. Such penetration of carbon into the active area results in degrading of the characteristics of the resulting semiconductor device, as is well known in the art. In view of this, the TEOS process is generally performed at a low temperature for formation of device isolation structures, and therefore, TEOS is not an acceptable replacement for the HTO process as claimed in the present invention.

In view of the above, it is submitted that the LP-TEOS process is unsuitable for densification of the underlying insulating layer in connection with the present invention, and therefore, for purposes of the present invention, does not represent an "art equivalent" of the HTO layer claimed in claim 1 of the present invention.

It is therefore submitted that the combination of the Laparra, Park, and Shin references fails to teach or suggest the present invention as claimed in independent claim 1. In particular, none of the references, alone, or in combination, teach or suggest "providing a high-temperature oxide (HTO) layer on the insulating layer" in a trench isolation process. Specifically, Laparra teaches providing a "continued application of a silica-based material" in an "HDP deposition" process to form coating 40b in a preferred embodiment (see Laparra, column 5, lines 6-11). Laparra also suggests application of a low-pressure chemical vapor deposition (LPCVD) of a TEOS-based dielectric, in an alternative embodiment (Laparra, column 5, lines 51-57). At the

same time, Park discloses application of a "PE-TEOS or PE-OX layer" as stress-relieving material layer 118 as a protection layer during subsequent plasma processing, and in no way used as in the present invention for the purpose of densification of an underlying insulating layer. Shin, while mentioning various compositions and application approaches for forming an "etch blocking layer" 127, has nothing to do with trench isolation, and is cited in the Office Action as supporting a temperature range for the LPCVD-TEOS film deposition process and mentions formation of an HTO layer.

In addition, none of the references, alone or in combination, teach or suggest densifying "the underlying insulation layer" ... "during formation of the HTO layer" as claimed in independent claim 1. Laparra makes no mention of any such densification of the underlying insulation layer 40a at all, let alone during formation of an "HTO layer", as claimed in amended claim 1. Park, on the other hand, teaches that a subsequent "annealing process is carried out" ... "in order to densify the USG layer" (Park, column 4, lines 66-67), a step that is not necessary in the process of the present invention, owing to the use of the HTO layer. Shin makes no mention of such densification, since Shin is not related to trench isolation. It is therefore submitted that the combination of references fails to teach or suggest the combined operation of forming an upper HTO layer, while, during its formation, densifying the underlying insulation layer.

In view of the above, it is submitted that the combination of Laparra, Park, and Shin fails to teach or suggest the present invention as claimed in independent claim 1. Accordingly, reconsideration of the rejection and allowance of claim 1 are respectfully requested. With regard to the various dependent claims 2 and 4-12, it follows that these claims should inherit the allowability of the independent claim from which they depend.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: June 26, 2003

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Version with Markings to Show Changes Made

In the specification:

The paragraph at page 5 line 12 through page 6 line 1 is amended above as follows:

(Amended) In order to prevent the inner wall of the trench 17 from additionally being oxidized, a silicon nitride [oxide] layer, i.e., oxidation barrier layer 20 is formed on an overall surface of the resulting structure where the oxide layer 19 is formed. It is preferable that a capping layer 21, for example, CVD oxide layer for protecting the oxidation barrier layer 20, is formed on the oxidation barrier layer 20. The capping layer 21 prevents damage of the oxidation barrier layer 20 in the following process for forming an insulating layer which fills a trench. Specifically, if the trench is filled with an HDP oxide layer, the capping layer 21 protects the oxidation barrier layer 20 from etching with argon. If the trench is filled with a USG layer instead of the HDP oxide layer, on an overall surface of the above resulting structure where the trench 17 is formed, plasma treatment is carried out to improve deposition characteristic of the USG layer. In this case, the oxidation barrier layer 20 may be damaged from plasma. The capping layer 21 prevents the damage of the oxidation barrier layer 20. The oxidation barrier layer 20 and capping layer 21 are formed to have a thickness of 20Å~300Å, respectively.

In the claims

Claim 10 has been amended as follows:

10. (Amended) The method of Claim 8, wherein the oxidation barrier layer comprises silicon nitride [oxide] with a thickness of 20Å~300Å.